DESIGN OF LOW POWER HALF SELECT FREE WRITE ASSIST 9T SRAM CELL USING TRIMODE MT-CMOS TECHNIQUE

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ABSTRACT:

Low power design has a vital role in the production of system on chips (SOC). So, every circuit is to be low power design, because High power consumption in portable electronics devices is an issue of serious concern. Shortening of battery life and additional packaging and cooling requirement are associated with high power consumption. The Static random-access memory (SRAM) is vastly used memory cell in consumer electronics. So, it is need to be an ultra-low power design. To obtain low power SRAM cell need to apply low power techniques. Firstly, Design the 9T SRAM cell check it's write and read operation for that 2x2 SRAM array is to be designed, after this initiate the implementation of low power techniques to the SRAM cell. Here two low power techniques are designed i.e. Multi Threshold-CMOS, Trimode MTCMOS using 90nm CMOS technology. The simulation results and graphical plots demonstrate the most suitable low power technique to reduce the dynamic power consumption of Half select free write assist 9T SRAM cell.

Keywords: CMOS, MTCMOS, trimode, 9T SRAM.

1. INTRODUCTION:

High power consumption in portable electronics devices is a serious problem. High power consumption is linked to reduced battery life, more packing, and cooling requirements. Complete power dissipation includes a crucial component known as static power dissipation caused by standby leak currents. A significant portion of the system's total power dissipation is accounted for by fixed power dissipation occurring in these idle components. Therefore, reducing this leakage component becomes essential for accurate power monitoring. The

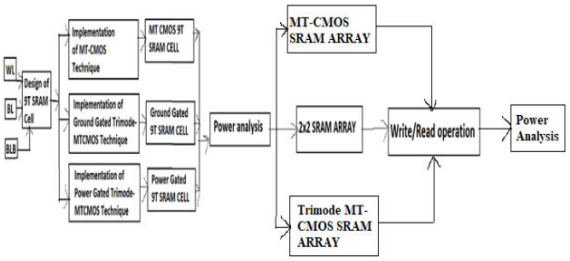
performance of MOS devices has actually improved significantly as a result of continued scaling of MOS tools. Due to leak currents, this has actually caused increased power dissipation. The drainpipe used to handle below-limit current has traditionally been the main leak point. Recent years have seen rapid and also creative advancements in low-power layout because to the growing importance of mobile systems and the need to restrict power consumption (and thus, heat dissipation) in very-high thickness ULSI chips. Mobile applications, such as laptop computers, mobile communication devices, and personal digital assistants, that need low power dissipation and high throughput are what are driving these improvements (Personal organizers). In the majority of these cases, it is necessary to achieve both the goals of high chip thickness and high throughput while also reducing power consumption. As a result, the low-power design of digital integrated circuits has emerged as a very active and quickly developing area of CMOS layout. Reduced power consumption in digital systems can be achieved using a wide range of approaches, from device/process level to formula level. Device characteristics, such as limit voltage, device geometries, and nearby dwellings are all important considerations in lowering power consumption. A growing range of personal computing devices, including mobile desktop computers, digital pens, audio and video-based multimedia products, cordless interaction and imaging systems, such as personal digital assistants, personal communicators, and smart cards, is the second force behind the low power design craze. These tools and systems necessitate complex performances, high-throughput computations, and often real-time refining capabilities. These devices' functionality is constrained by the size, weight, and battery life. The IC design community has been looking more intently lately for brand-new techniques and approaches that create more power-efficient styles, which implies significant reductions in power consumption for the same level of performance due to severe reliability issues, increased style costs, and battery-operated applications. Memory circuits, whether they be Dynamic RAMs, Fixed RAMs, Ferroelectric RAMs, ROMs, or Flash Memories, become an essential component of any system design and significantly increase the system's level of power consumption. It is possible to significantly increase system power-performance, performance, integrity, and costs by reducing the power dissipation in memories. Due to the increased demand for notebooks, laptops, handheld interface devices, and IC flash memory cards, RAMs have seen a remarkably quick progress in low power, low-voltage memory design in recent years. Leakage current is one of

the major challenges with typical CMOS SOCs. Leakage is an ongoing problem that is especially important because it eliminates the low-power advantages of the CMOS circuits that we currently take for granted. It is clear that the leak current increases by several orders of magnitude as the technology advances. Later years' revised predictions show an even larger increase. Because it is closely related to temperature, the leakage present poses a major risk for applications with the capacity to operate at high temperatures. According to this, the leakage current is the main cause of the Intel Pentium processors' sleep power consumption, and efforts are being made to reduce this current using new technology and circuit techniques. Historically, measures have been taken to reduce the high subthreshold leak current and keep overall leakage levels within acceptable ranges for high-performance processors.

2. RELATED STUDY:

Each bit is stored using bi-stable latching circuitry in a type of semiconductor memory known as fixed random-access memory (static RAM or SRAM) (flip-flops). Although SRAM shows data durability, it is nonetheless volatile in that data finally vanishes when the memory is turned off. The term static random-access memory (SRAM) distinguishes it from DRAM (vibrant random access memory), which needs to be periodically refreshed. Because SRAM is both quicker and significantly more expensive than DRAM, it is frequently used for CPU cache instead of main memory. The popularity of Fixed Random Access Memory (SRAM) and CMOS technology scaling in different processors and system-on-chip (SoC) devices has fueled the desire for improvement in the field of SRAM design. Since SRAM bit cells are created with the barest minimum of geometry tools for high thickness and to keep up with CMOS innovation scaling, they are the first to experience side-effects brought on by technology scaling. However, how well SRAM is comprehended will determine how well the next generation of technology succeeds. Alternative SRAM bit cell topologies and range designs have so lately been proposed as solutions to the Nano-regime problems. The key difficulties in SRAM design are inadequate security, process variation tolerance, tool degradation from ageing and soft errors, to name a few. Fixed random-access memory (SRAM) is widely used in mobile devices, System On-Chip (SoC), and high-performance VLSI

circuits, which is driving up SRAM demand. SRAM occupies approximately 70% of the System on Chip. SRAM is an essential component found in numerous commercial and industrial subsystems, automotive electronics, and CPUs. Additionally, it can be utilised as a cache memory in microcontrollers, portable devices, and external ruptured configuring SRAM caches. The Cadence device was used to create the SRAM cell, which employs 90nm CMOS technology and functions as a typical basis for the construction given directly to the construction unit. When constructing the SRAM circuit, it is essential to effectively complete the read and create operations. The following are the SRAM's fundamental parts: 20 The realisation that dependable and durable parts lead to a long system operational life is the fundamental advantage of preventing part strain during power-up. Large capacitors are used in the input circuit of the controller that regulates the current flowing through the electric motor. Signal processing and communication in electronic devices are generally regarded to have become conscious to the buyer. The SRAM memory cell is the basic component of the SOC (System on chip). The storing element of a memory is known as a cell. The storage region is often referred to as the memory area. The developer therefore needs pricey tools and a system that minimises form factor. The developer therefore adds SOC Designing. This has an SRAM cell that occupies 70% of the space of the SOC. The operation then demands a modest power level. Which is crucial for the design of the SRAM type memory cell now in use since it is in high demand on the professional level of the market? However, this does require a substantial amount of functioning and a strong design. But make sure the market and the designer are well acquainted. 3.1.1 SRAM CELL this cell is referred to as fixed random-access memory. Its operation has a big impact on the memory layout work done by the developer. The process supports bit-oriented and word-oriented parameters. The majority of electronic devices use the SRAM, a heavily used electrical component. These tools are frequently used for commercial and non-commercial markets. An SRAM is made to satisfy two crucial requirements. They are. 1. It offers a direct connection to the CPU (a key refiner) at rates that DRAMs are unable to match. 2. To replace DRAMs in extremely low-power devices.



9T SRAM cell:

Two cross-coupled CMOS inverters, four access transistors, one read discharge transistor, and other components make up the 9T SRAM cell. The interior nodes of the cell are built using the output (input) of the inverters. Gain access transistors aid in the communication between the cell's input/output ports and internal nodes. Bit lines are the name for the cell's input and output ports (BL as well as BLB). Create a procedure. As shown in the following number, the checked discharge (RD) transistor is OFF during the creation process. When the bit line (BL) is low and the tiny bit line bar (BLB) is high, the second inverter's input is high and its output is low. The output QB and result of the second inverter's input to the first inverter are both high.

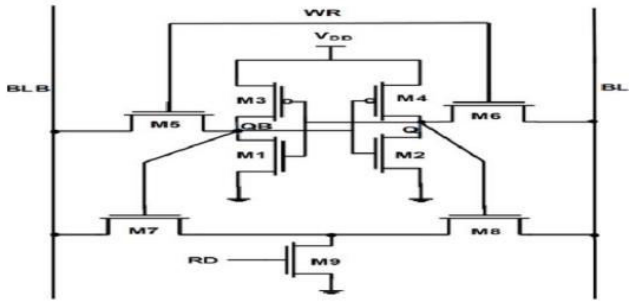


Fig.1. Model diagram.

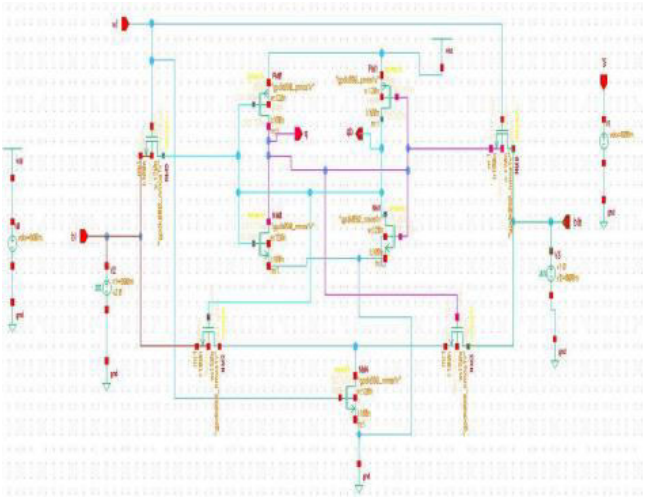


Fig.2. Schematic of 9T SRAM Cell.

The read discharge (RD) transistor activates when the checked out method receives the lower value. Both the bit line and the tiny bit line bar are pre-charged to VDD. depending on data held in bits at nodes QB and Q. Depending on whether the QB is high, bit line bar (BLB) or bit line (BL) are discharged to the ground.

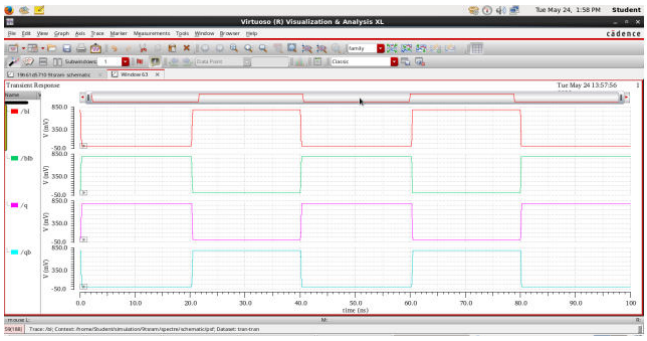


Fig.3. Simulation result of transient analysis for 9T SRAM Cell.

Fig.4. Simulation results of Power Consumption for 9T SRAM Cell.

SINGLE ENDED 9T SRAM CELL:

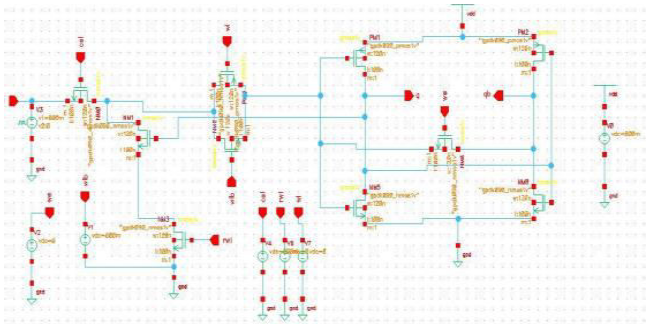


Fig.5. Schematic of Single ended 9T SRAM Cell.

The BL was pre-charged to VDD during the read procedure. When CSL (column selection control line), N5 (read discharge transistor), and RWL (read word line) turn on, the bit line (BL) starts discharging to ground via a path established by CSL, N5, and RDT (read discharge transistor), as shown in the preceding number. If node QB is negative, a little amount of line BL is recharged to VDD. After that (bit line) when QB is one, BL discharges to ground.

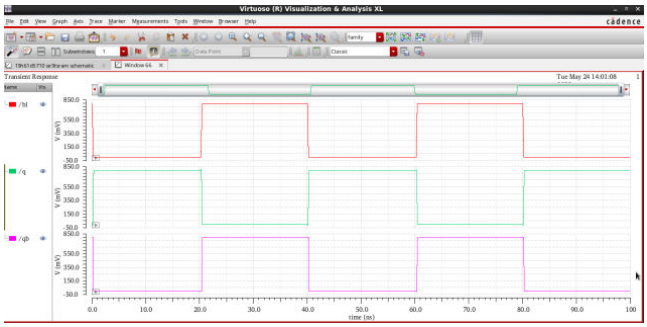


Fig.7. Simulation result of transient analysis for Single ended 9T SRAM Cell.

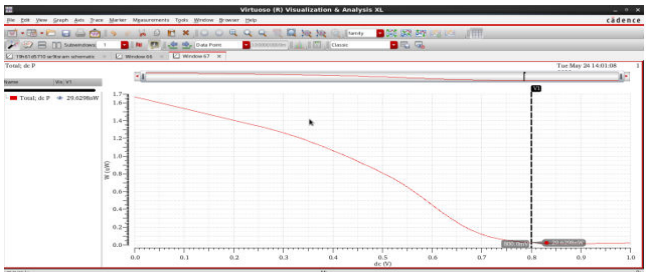


Fig.8. Simulation result of Power Consumption for Single ended 9T SRAM Cell.

TRANSMISSION GATE 9T SRAM CELL:

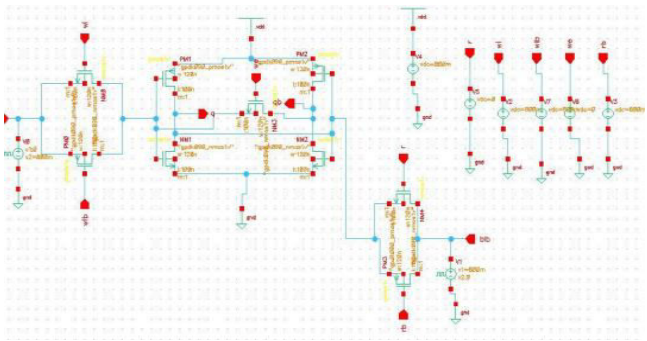


Fig.9. Schematic of Transmission Gate 9T SRAM Cell.

WE is wired to ground during the compose process to avoid a half-select problem (compose enable). Because bit line (BL) is low in the circuit above, word line (WL) is connected to high and Q is linked to reduced. First inverter input is high, causing Q to be low. The second inverter's input is low and the output quality is high as a result of the first inverter serving as its input. Only Transmission gate TG1 enters, while Transmission entry TG2 is off. Finally, we can enter one within the cell. QB will follow when Q2 BLB is low. Once more, when the output of the second inverter is used as its input, the results are subpar. We are finally able to type no into the cell.

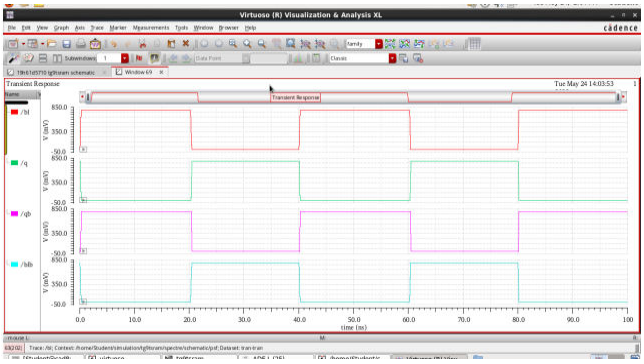


Fig.10. Simulation result of transient analysis for Transmission Gate 9T SRAM Cell.

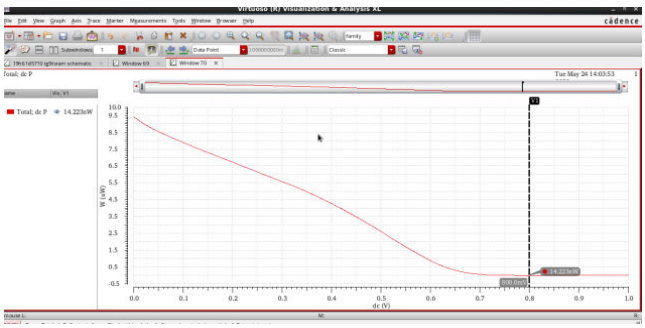


Fig.11. Simulation result of Power Consumption for Transmission Gate 9T SRAM Cell.

HALF SELECT FREE WRITE ASSIST 9T SRAM:

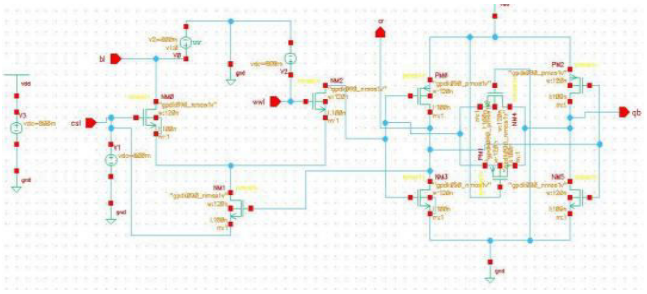


Fig.12. Schematic of Half select free write assist 9T SRAM cell.

The (write allow) WE and the (create allow bar) WEB are connected to high during the writing process to avoid a fifty-fifty choice problem. Along with WE, which is connected to low in the circuit, BL, CSL, WWL, WEB, and VGND are all connected to high and low, respectively, in the diagram. Here, the input is high and the first inverter's output QB is low. Second inverter input is reduced by first inverter output feeding into it, improving result Q. Finally, we can enter one within the cell. When CSL, WWL, WEB, VGND, and WE, BL connected to high and low, respectively. Below, the initial inverter input is low, and as a result, QB is high. The output of the first inverter serves as the input for the second inverter once more because the result Q is low. Finally, we may just enter 0 into the cell directly.

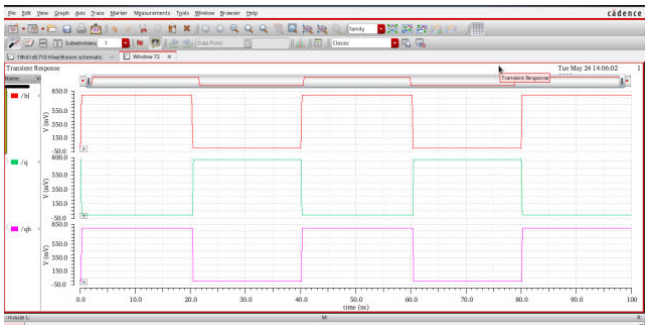


Fig.13. Simulation result of transient analysis for Half select free write assist 9T SRAM cell.

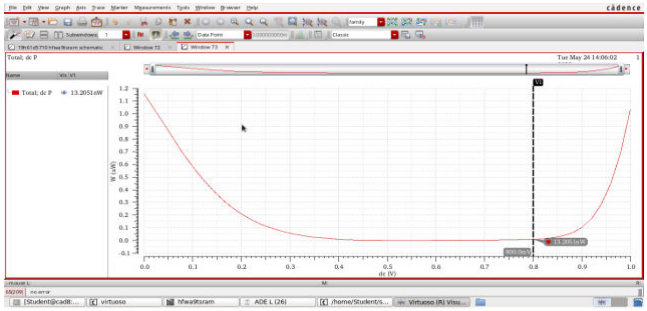


Fig.14. Simulation result of Power Consumption for Half select free write assist 9T SRAM cell.

HALF SELECT FREE WRITE ASSIST 9T SRAM CELL USING MTCMOS TECHNIQUE:

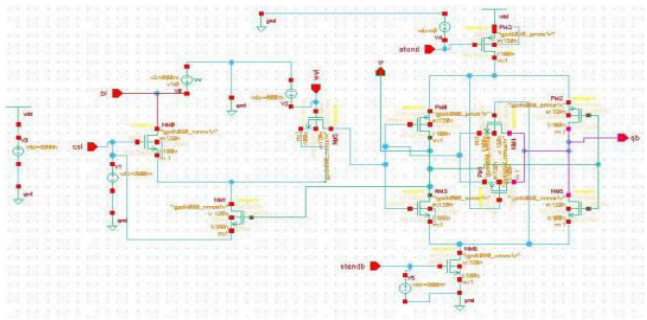


Fig.15. Schematic of MT-CMOS Half select free write assist 9T SRAM cell.

The crucial component of MT-CMOS is its use of the remaining transistors to maximise power efficiency. - These sleep transistors are used to build the logic-supplying online power rails. The physical power rails are connected to the online power rails using high Vt Rest transistors.

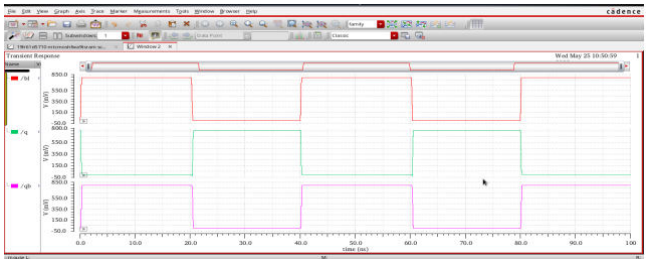


Fig.16. : Simulation result of transient analysis for MT-CMOS Half select free write assist 9T SRAM cell.

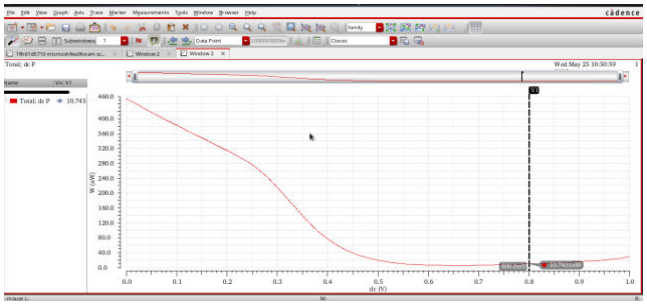


Fig.17. Simulation result of Power Consumption for MT-CMOS Half select free write assist 9T SRAM cell.

HALF SELECT FREE WRITE ASSIST 9T SRAM CELL USING GROUND GATED TRIMODE MT-CMOS TECHNIQUE:

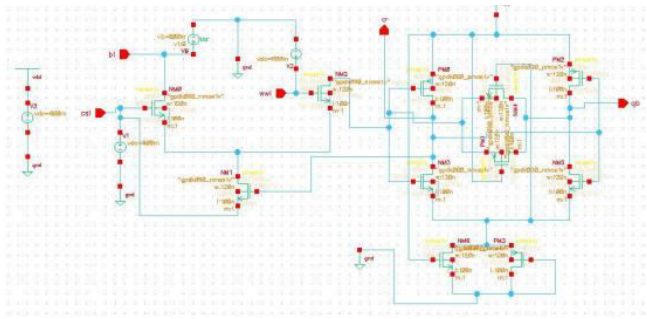


Fig.18. Schematic of Half select free write assist Ground Gated Trimode MT-CMOS Technique.

In order to prevent the fifty-fifty pick problem, WE is connected to ground during the writing process, whereas WEB is connected to high. In the circuit above, VGND is joined to high in the BL (column option control line), CSL (create word line), WWL (word line), WEB (ground), and WE is connected to low. First inverter input is high below it, and output QB is likewise decreased. The output of the first inverter serves as the input for the second, resulting in a lower second inverter input and a high output Q. We can finally insert one into the cell. When WE, BL connected to low and CSL, WWL, WEB, VGND connected to high. First inverter input is low below, and QB is a high result. Once more, the output of the first inverter serves as the input for the second inverter, reducing Q as a result. In the end, we have no right to build anything inside the cell.

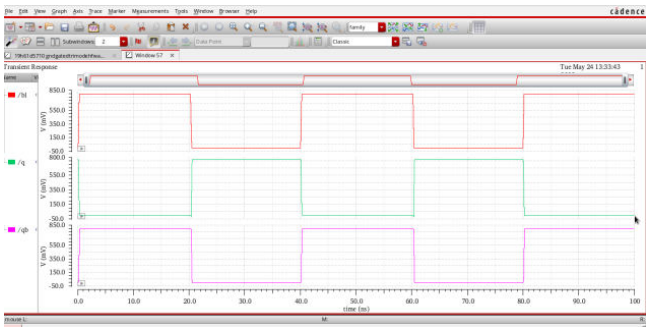


Fig.19. Simulation result of transient analysis for Ground Gated Trimode MT-CMOS Half select free write assist 9T SRAM cell.

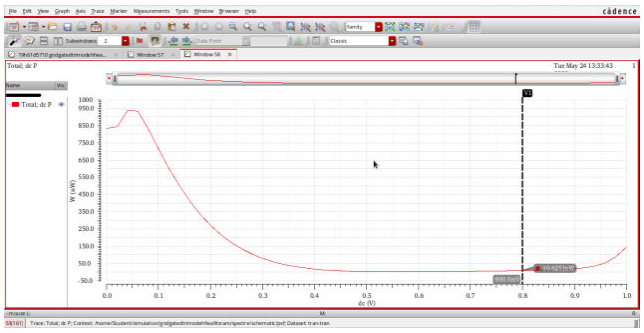


Fig.20. Simulation result of Power Consumption for Ground Gated Trimode MT-CMOS Half select free write assist 9T SRAM cell.

HALF SELECT FREE WRITE ASSIST 9T SRAM CELL USING POWER GATED TRIMODE MT-CMOS TECHNIQUE:

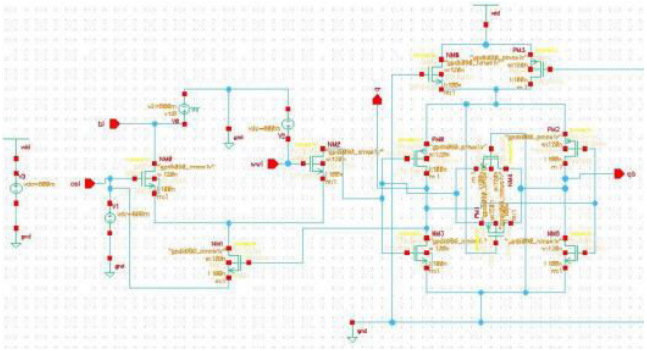


Fig.21. Schematic of Power Gated Trimode MT-CMOS Half select free write assist 9T SRAM cell.

In order to prevent a fifty percent pick issue, WE is connected to the ground during write operations, and internet is connected to the highest point. In the circuit above, WE is connected to low while VGND is attached to high for the column selection control line, CSL, generate word line, Internet, and ground. Here, the initial inverter input is high but the output QB is low. The output Q is high and the second

inverter input is reduced as a result of the initial inverter's input action. We can finally enter one inside the cell. When WE, BL and CSL were connected to low and WWL, Internet, VGND, high, respectively. Here, the first inverter input is low, and the result QB is high. Once more, the result of the first inverter's input for the second inverter and the result Q are both poor. Finally, we may enter the word "no" into the cell.

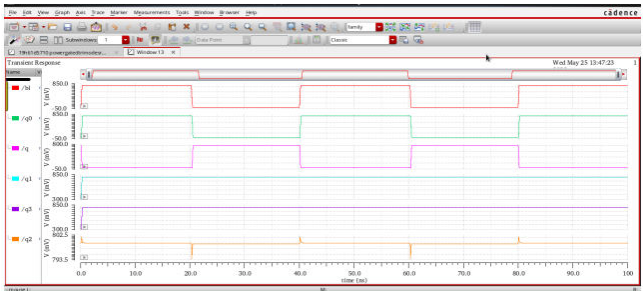


Fig.22. Simulation result of transient analysis for Power Gated Trimode MT-CMOS Half select free write assist 9T SRAM cell.

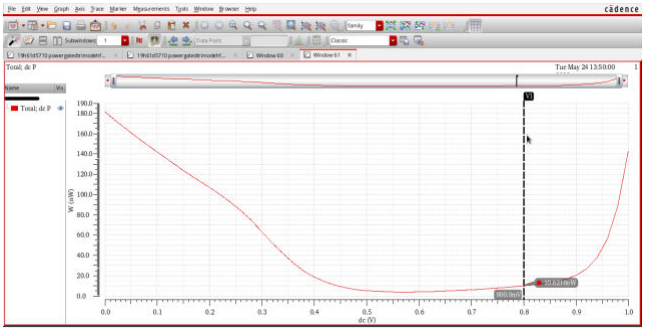


Fig.23. Simulation result of Power Consumption for Power Gated Trimode MT-CMOS Half select free write assist 9T SRAM cell.

SRAM CELL	power
9TSRAM	49.5µW
Single Ended 9T SRAM Cell	29.62nW
Transmission Gate 9T SRAM Cell	14.22nW
Half Select Free Write Assist 9T SRAM Cell	13.2051nW
Half Select Free Write Assist 9T SRAM Cell MTCMOS Technique	10.74nW
Half Select Free Write Assist 9T SRAM Cell Ground gated Trimode MTCMOS Technique	10.625nW
Half Select Free Write Assist 9T SRAM Cell Power gated Trimode MTCMOS Technique	10.621nW

2X2 SRAM Memory Array:

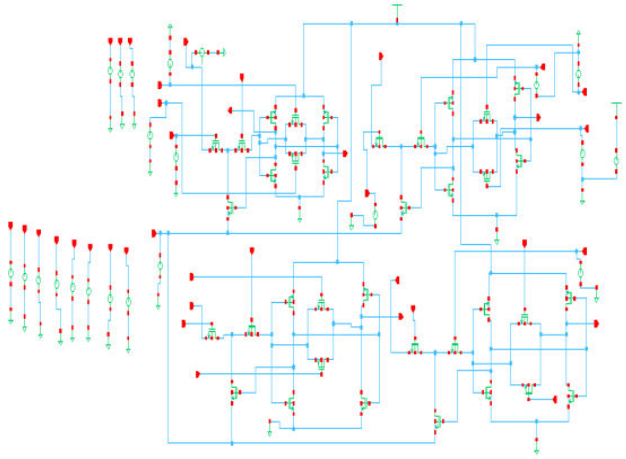


Fig.24. Schematic of 2x2 SRAM Array when it selects S0.

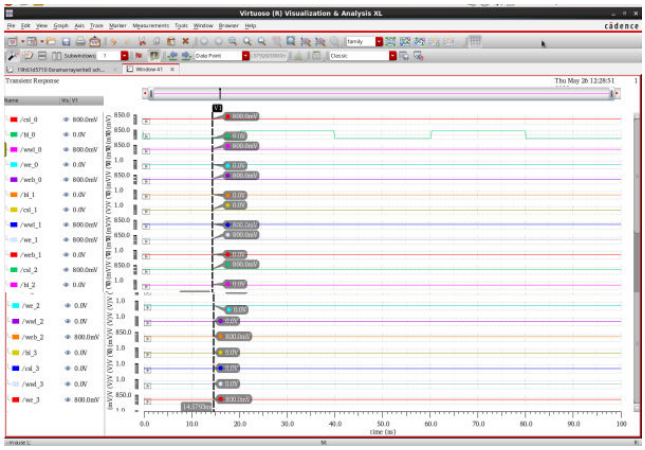


Fig.25. Simulation result of transient analysis for 2x2 SRAM Array when it selects S0 write 0 operation.

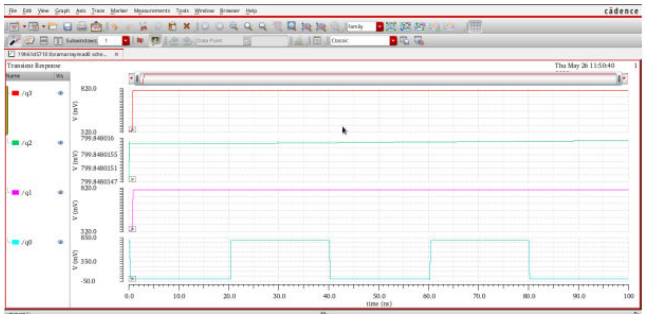


Fig.26. Simulation result of transient analysis for 2x2 SRAM Array when it selects S0 read 0 operation.

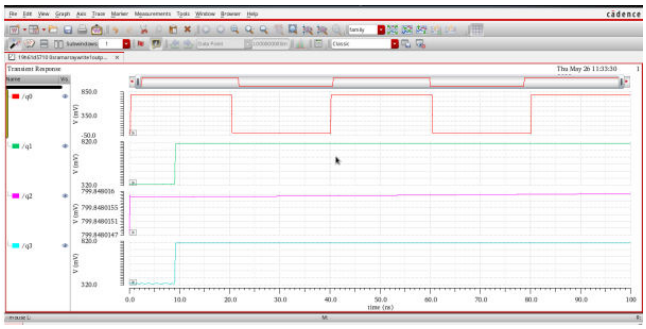


Fig.27. Simulation result of transient analysis for 2x2 SRAM Array when it selects S0 read1 operation.

2X2 SRAM ARRAY WITH MTCMOS:

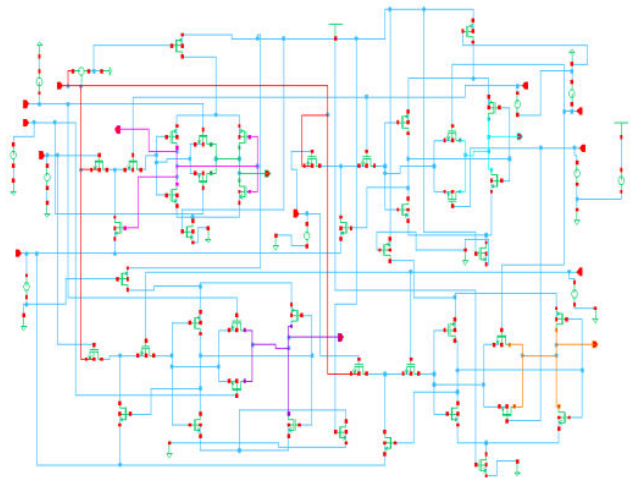


Fig.28. Schematic of 2x2 SRAM Array with MT-CMOS when it selects S0.

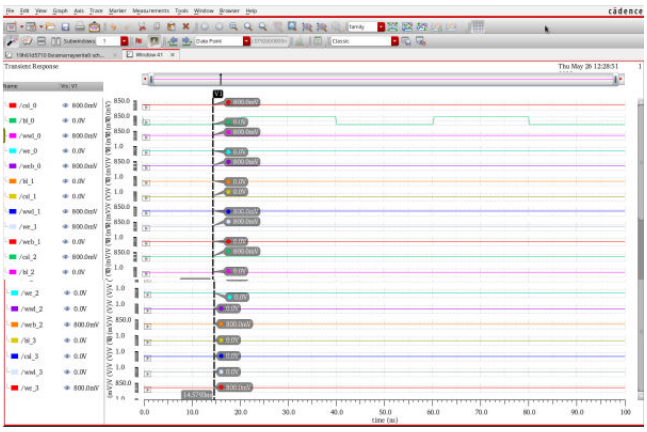


Fig.29. Simulation result of transient analysis for 2x2 SRAM Array with MT-CMOS when it selects S0 write 0 operation.

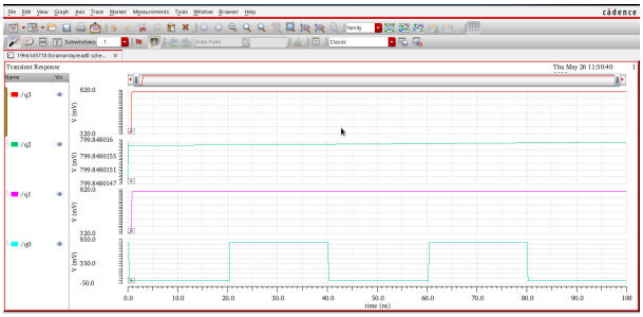


Fig.30. Simulation result of transient analysis for 2x2 SRAM Array with MT-CMOS when it selects S0 read 0 operation.

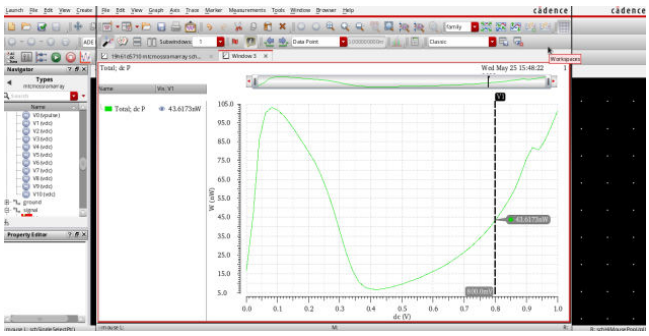


Fig.31. Simulation result of Power Consumption for 2x2 SRAM Array with MT-CMOS.

2X2 SRAM ARRAY GROUND GATED TRIMODE MT-CMOS:

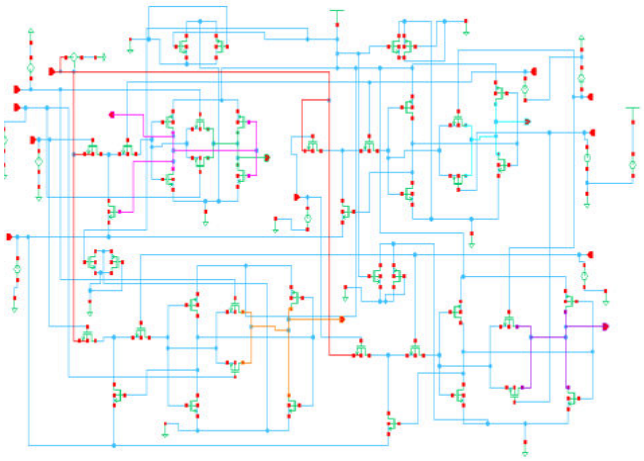


Fig.32. Schematic of 2x2 SRAM Array with GROUND GATED TRIMODE MT-CMOS when it selects S0.

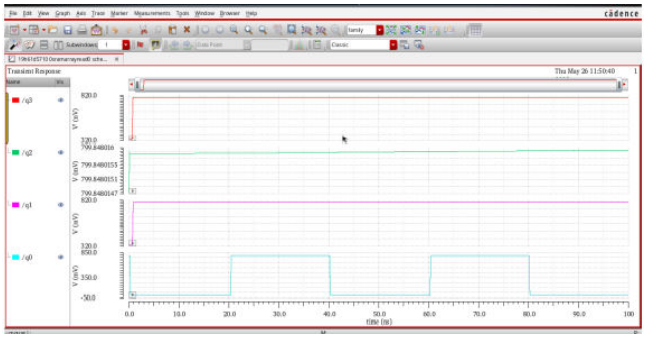


Fig.33. Simulation result of transient analysis for GROUND GATED TRIMODE MT-CMOS when it selects S0 read 0 operation.

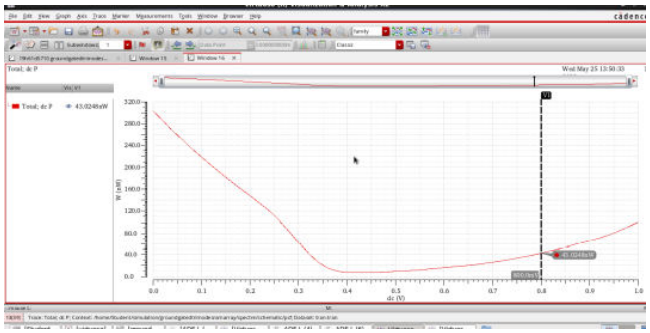


Fig.34. Simulation result of Power Consumption for 2x2 SRAM ARRAY GROUNDGATEDTRIMODE MT-CMOS.

2X2 SRAM ARRAY POWER GATED TRIMODE MTCMOS:

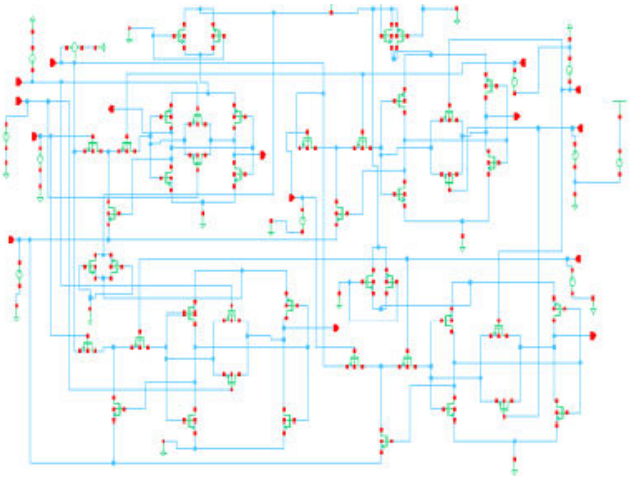


Fig.35. Schematic of 2x2 SRAM Array with POWER GATED TRIMODE MT-CMOS when it selects S0.

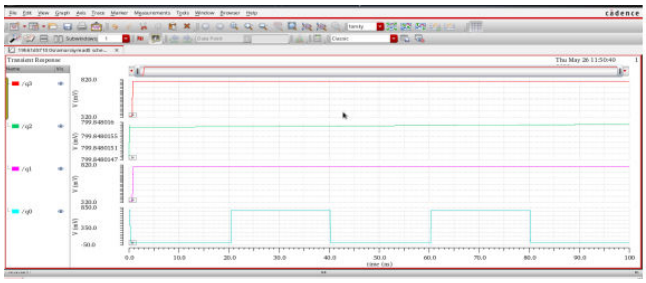


Fig.36. : Simulation result of transient analysis for POWER GATED TRIMODE MT-CMOS when it selects S0 read 0 operation.

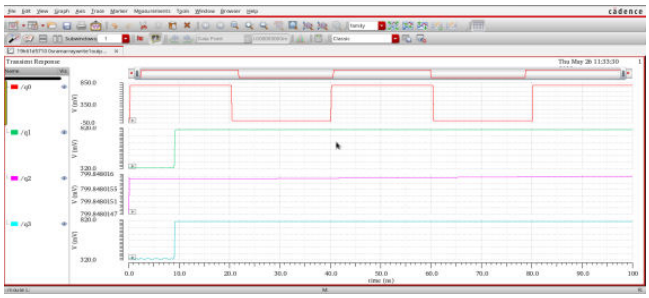


Fig.37. Simulation result of transient analysis for POWER GATED TRIMODE MT-CMOS when it selects S0 read1 operation.

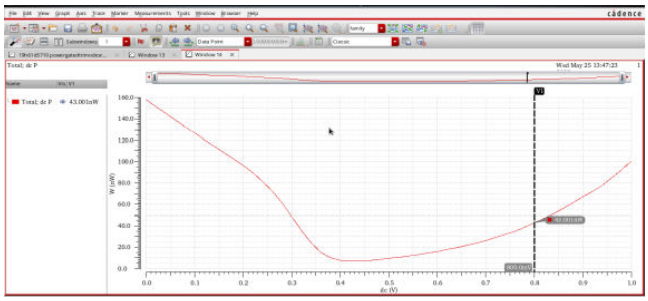


Fig.38. Simulation result of Power Consumption for 2x2 SRAM ARRAY POWER GATEDTRIMODE MT-CMOS.

COMPARISON OF POWER CONSUMPTION:

SRAM ARRAY	POWER
2X2 SRAM ARRAY	47.09nW
2X2 SRAM ARRAY WITH MT-CMOS TECHNIQUE	43.61nW
2X2 SRAM ARRAY WITH POWER GATED TRIMODE MT-CMOS TECHNIQUE	43.001nW
2X2 SRAM ARRAY WITH GROUND GATED TRIMODE MT-CMOS TECHNIQUE	43.02nW

CONCLUSION

A 9T SRAM memory cell with Low Power 50% Select Free Compose Support is created. For that, we investigated low-power technologies including MULTI-THRESHOLD CMOS, Trimode MT-CMOS, and Half-Choice Free Write Support 9T SRAM Memory Cell. It is necessary to confirm that the create and review operations for the 50% pick free create help 9T SRAM memory cell are functioning properly before implementing these low power strategies. To comprehend this, we must build a 2x2 SRAM Memory Array that can store 4 bits of data. The SRAM memory cell's supply voltage is 800.0 mV. By reflecting on the results we saw When compared to a 9T SRAM memory cell with half pick free create assistance, the power utilization of the power gated trimode MT-CMOS technique can be reduced to just 37%. Following the creation of this 2x2 SRAM choice for 4-bit data storage. The Cadence Virtuoso device uses 90nm technology to build the SRAM variation, SRAM cells, and essential components.

PROJECTED EXTENSION:

The major focus of this work is obtaining the low power Half Choose Free Compose Assist 9T SRAM Cell using low power techniques. Only 2 power strategy efficiencies were taken into account in this optimization procedure and were verified in the CAD devices such as tempo for that specific area. This 9T SRAM Cell with maximized low power 50% pick-free creation assistance can be used in emerging modern technologies like IOT-based tools and Expert system-based systems. Due to its low leakage and low power characteristics, this optimized low power memory cell will be in great demand in the next decades.

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